REMARKS

Claims 33-55 have not been amended, and are still pending in the present application.

Claims 33-55 stand rejected under either 35 USC 103(a) as being unpatentable over USP 5,574,475 to Callahan, Jr. et al. ("Callahan") in view of the Applicant's admitted prior art ("APA"). These rejections are respectfully traversed.

Claims 33, 39, 46, 51

For independent claims 33, 39, 46, 51, the Examiner acknowledges that Callahan does not disclose "a driver circuit that comprises a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output, each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines". To compensate for these missing limitations in Callahan, the Examiner has asserted that FIG. 3 of the APA discloses all of these limitations, and that it would be obvious to modify Callahan's system with that of the APA.

First, it is well-known that the prior art must contain a teaching or suggestion to make the proposed modification. In this regard, there is no teaching or suggestion in either Callahan or APA to make the proposed modification.

Second, Applicant respectfully submits that it be improper to modify Callahan with the teachings from the APA because the ***proposed modification would change Callahan's principle of operation***. It is well-known that, if the proposed modification of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. See *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

The driver circuit in FIG. 7 of Callahan operates based on NAND operations, as illustrated in FIGS. 3A and 6, and column 11, line 46 to column 12, line 25. In contrast, FIG. 3 of the APA operates based on a decoding scheme. Therefore, simply substituting the transistor-layout of FIG. 3 into the driver circuit in FIG. 7 of Callahan will render the driver circuit in Callahan to be non-operative because it would ***change the principle of operation*** of the driver circuit of FIG. 7 in Callahan. For example, in Callahan, when each switch is regarded as a transistor in a decoder circuit, the switch outputs a desired voltage level according to a result of the NAND operation. However, the transistors in the APA output a desired voltage level according to the signals on the digital signal lines,

which is not a logic operation. In this regard, note that none of the NAND gates in FIG. 3A of Callahan receive any voltage levels.

In other words, modifying FIG. 7 of Callahan with FIG. 3 of the APA will change the principle of operation of FIG. 7 of Callahan, and possibly render the resulting circuit to be non-operative. At a minimum, significant re-design of the FIG. 7 circuit will be needed to incorporate the circuit of FIG. 3 of the APA. This can only be accomplished by ***impermissible*** hindsight reconstruction. Thus, the APA cannot be combined with Callahan to support the rejection.

Claim 46

The Examiner further acknowledges that Callahan does not disclose a circuit where the number of the plurality of digital signal lines on the first side of the output is equal to 2n-2. However, the Examiner asserts that it would be obvious to choose the number of inputs in Callahan to be an odd number (such as 5 bit inputs) so as to meet this limitation.

Applicant respectfully submits that claim 46 is allowable to begin with based on the reasons set forth above. Given the significant modifications that are already needed to incorporate FIG. 3 of the APA into FIG. 7 of Callahan, it would be even more far-fetched to suggest that the ***modified*** circuit can be ***further modified*** to meet the limitations set forth in claim 46. Applicant respectfully submits that this further modification can only be the result of ***impermissible*** hindsight reconstruction. In addition, there is no teaching or suggestion in either Callahan or APA to make the proposed modification.

Claim 51

The Examiner further acknowledges that Callahan does not disclose a circuit that has at least one level-shifter, with each level-shifter associated with a digital signal line. However, the Examiner asserts that the inverter 124 in FIG. 7 of Callahan corresponds to the claimed level-shifter because it causes its input to shift, citing column 2, lines 1-13 of Callahan.

Applicant respectfully submits that the inverter 124 cannot correspond to the claimed level-shifter. First, column 2, lines 1-13 of Callahan do not expressly state that the inverter 124 performs level shifting. Second, given the context in which the inverter 124 is used for FIG. 7, it is not clear that the inverter 124 actually performs level shifting. In fact, the box 124 in FIG. 7 represents the inverter 104 and the switch 108 in FIG. 6 (see column 12, lines 5-7), which do not appear to be performing any level shifting.

Claims 38 and 45

Applicant respectfully submits that dependent ***claims 38 and 45*** define additional patentable subject matter. Claims 38 and 45 recite that each transistor group has a total of m transistors, with m being a positive integer that is greater than n. Since independent claims 33 and 39 already recite that there are n controllable transistors in each transistor group, claims 38 and 45 essentially recite that there is at least one (i.e., m-n) transistor in each transistor group that is not a controllable transistor. This is supported, for example, by FIG. 5 of the present application, where there are two non-controllable transistors coupled between the output and voltage level V0. In contrast, all the transistors (e.g., 110, 112 in FIG. 7) in Callahan are controllable transistors.

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In light of the above, all pending claims are submitted to be in condition for allowance. Reconsideration and allowance of this application is respectfully solicited. The Examiner is invited to telephone the undersigned if there are any amendments or issues that can be resolved in a phone conversation.

Respectfully Submitted,

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CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal service as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Date: September 7, 2005 By: _____
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